REMARKS

Claims 1, 11, 12, 13, and 20 are amended, no claims are canceled, and no claims are added; as a result, claims 1-20 are now pending in this application.

§112 Rejection of the Claims

Claims 1-20 were rejected under 35 U.S.C. § 112, first paragraph. In rejecting claims 1-20, the Office Action states, "The claim contains subject matter which was not described in the specification and such a way as to enable one skilled in the art to which it pertains, or with which it is most merely connected, to make and/or use the invention."[1] Applicant respectfully submits that the Instant Application meets the requirements of U.S.C. § 112, first paragraph because the Instant Application includes a specification that describes the claimed subject matter in a manner that is enabling to one of ordinary skill in the art. In the rejection, the Office Action asserts that claim 1 and the specification describe an encoding method that cannot address every location within a memory page. The Office Action states,

> "Since first bit is only set to zero in this case, offset (0 to 12 bits) can only access half of the address that starts with 0, because bit 12 is always 0 for 8KB page size. Likewise, for 16 KB page size example in Fig. 5C, since bit 13 and 12 is set to zero and one respectively, offset (0 to 13 bits) can only access the quarter of the address that starts with 01 and unable to access any address starts with 00, 10, or 11."[2]

Applicant submits that the Office Action misunderstands Applicant's claims and specification. Applicant points-out that the Instant Application's specification describes TLB entries that include a virtual address encoded with a page size, while also describing virtual addresses that are not encoded with a page size. In particular, Figure 2, Figure 4A, and their associated text[3] describe *inter alia* virtual addresses that are not encoded with a page size. Figures 5A, 5B, 5C, 6, and their associated text[4] describe *inter alia* a method of encoding a page

[1] Office Action mailed November 5, 2005 at page 2.
[2] *Id.*
[3] For text associated with Figure 2, see Instant Application at page 6, line 22 to page 8, line 7. For text associated with Figure 4, see Instant Application at page 6, line 22 to page 8, line 19 to page 9, line 6.
[4] For text associated with Figures 5A, 5B, 5C, and 6, see Instant Application at page 10, line 18 to page 13, line 8.

size within a virtual address. Figures 7, 8, and their associated text[5] go on to describe embodiments for looking-up a virtual address, which is not encoded with a page size, in a TLB whose entries are encoded with a page size.

Applicant submits that the above-noted portions of the specification provide an enabling disclosure for each and every feature of claims 1-20. In the claims, claim 1 recites a method for determining whether a virtual address is stored in a translation lookaside buffer (TLB). According to claim 1, the virtual address includes a first bit string, while the TLB includes a plurality of entries. The TLB entries include a minimum virtual page number bit string and a variable bit string. Claim 1 states, "if the first bit string matches the minimum virtual page number bit string, decoding a page size *stored in the variable portion of the matching entry* and *a 1-bit field associated with the matching entry.*"[6] Applicant points-out claim 1 does not indicate that the virtual address is encoded. Instead, claim 1's decoding occurs vis-à-vis data in a TLB entry Therefore, each and every feature of claim 1 is supported by an enabling description in the specification. Claims 2-19 are similarly supported.

For at least the reasons set forth above, Applicant submits that the Instant Application's specification provides an enabling description for claims 1-20.

Claims 12, 13, and 20 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 12, 13, and 20 to recite "a current page size." Applicant submits that this amendment overcomes this rejection.

Claims 13 and 20 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 13 and 20 to recite "less than," as noted in the Office Action. Applicant submits that this amendment overcomes this rejection.

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[5] For text associated with Figures 7 and 8, see Instant Application at page 13, line 12 to page 16, line 6.
[6] Instant Application at claim 1.

§103 Rejection of the Claims

Claims 1-5, 11, and 14-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mathews (U.S. Patent No. 6,625,715) and Kalyanasundharam (U.S. Patent No. 6,549,997). Applicant submits that the Office Action has not established a *prima facie* case of obvious vis-à-vis claims 1-9, 1-4, 6-13, 15-16, 19-22, 24-31 and 33-34.

> The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.[7]

Applicant submits the Office Action has not established a *prima facie* case of obvious because (1) the Office Action's combination does not teach each and every element of each rejected claim, and (2) the Office Action does not identify a motivation for combining the cited references. The discussion below will address these issues.

THE COMBINATION DOES NOT TEACH OR SUGGEST ALL ELEMENTS OF EACH CLAIM

Applicant submits that the Office Action's combination of Mathews and Kalyanasundharam does not teach or suggest each and every element of claims 1-20. For example, claim 1 recites, "the TLB including a plurality of entries, wherein the entries include a minimum virtual page size bit string and a variable bit string." Claim 1 further recites, "decoding a page size stored in the variable bit string of the matching entry and a data field associated with the matching entry." Therefore, claim 1's TLB entries include a page size in the

[7] M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

variable bit string of the matching TLB entry and a data field associated with the matching TLB entry.

Applicant submits that the combination of Mathews and Kalyanasundharam does not teach the claim features noted above. In particular, Mathews' Figure 7 shows a TLB whose entries include six fields (virtual address tag 742, page mask 744, physical page address 746, virtual address tag 752, page mask 754, and valid field 756[8]), none of which include a page size stored in the TLB entry's variable bit string, as recited in claim 1. Mathews is entirely different from claim 1 because Mathews' page size is not stored in Mathews' TLB entries. Instead, Mathews stores page sizes in a page size bias register 720, which is not part of the TLB's entries. In rejecting claim 1, the Office Action asserts that Mathews' valid field 756 includes part of the page size.[9] However, Mathews' describes the valid field 756 as "an indicator of the validity of the entry."[10] Thus Mathews' valid field 756 does not include part of the page size, as recited in claim 1.

The Office Action admits that Mathews does not teach or suggest "decoding a page size stored in the variable bit string of the entry,"[11] so the Office Action looks to Kalyanasundharam to provide what Mathews is lacking. However, as noted above, the combination lacks more than this, as Mathews' valid field 756 does not include part of a page size. Therefore, for the combination to teach or suggest all the elements of claim 1, Kalyanasundharam must teach or suggest claim 1's "decoding a page size stored in the variable bit string of the matching entry and a 1-bit field associated with the matching entry." The Office action points-to Kalyanasundharam's passages at column 5, lines 49-55 and column 6 lines 13-22 as supporting the rejection. The passage at column 5, lines 49-55 states,

> A representative page table entry (PTE) 206 in RAM 204 preferably stores a validity bit ("V") 208, a first size-field bit ("SZ[0]") 210, physical address bits ("PA[13:15]") 212 associated with SZ[0] 210, a second size-field bit ("SZ[1]") 214, physical address bits ("PA[16:18]") 216 associated with SZ[1] 214, a third size-field bit ("SZ[2]") 218, physical address bits ("PA[19:21]") 220 associated with SZ[2] 218, physical address bits ("PA[22:46]") 222 and status bits ("STATUS[8:0]") 224.

The passage at column 6, lines 13-21 states,

[8] Mathews discusses the TLB fields at column 9, line 22 to column 10, line 14.
[9] See Office Action mailed 10/05/2005 at page 5.
[10] Mathews at column 9, lines 36-38.
[11] Office Action mailed 10/05/2005 at page 5.

> FIG. 3A depicts a table 300 showing one system for encoding size-field data for the four different page sizes preferably supported by TLB 200 of FIG. 2. In contrast to the 2-bit encoding system embodied in the table of FIG. 1A, the page size data of FIG. 3A is represented by size-field data consisting of 3-bits. More generally, the present invention can support virtually any number of page sizes N by utilizing N-1 size bits (or cells) and associating therewith N-1 corresponding physical address bit (or cell) groups. Other encoding systems could also be utilized.

While these passages describe encoding page sizes, Applicant submits that they do not teach or suggest "a page size stored in the variable bit string of the matching entry and a 1-bit field associated with the matching entry," as recited in the claim 1.

For reasons similar to those noted above, Applicant submits that the Office Action has not made a *prima facie* case of obviousness for all the other claims rejected under 35 USC 103.

THE OFFICE ACTION HAS NOT PROVIDED A MOTIVATION TO MODIFY THE REFERENCES

The Office Action asserts that one of ordinary skill in the art would have combined Mathews and Kalyanasundharam for "a faster dynamic variable page size translation of addresses."[12] Although a faster dynamic variable page size translation of addresses may be desirable, such a desire is not enough to motivate one to modify Mathews and Kalyanasundharam as set-out in the Office Action. The Office Action does not point to any passages in the references that teach or suggest the Office Action's modifications. Therefore, Applicant submits that the Office Action has improperly combined Mathews and Kalyanasundharam.

[12] [12] See Office Action mailed 10/05/2005 at pages 5-6.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 6 day of February, 2006.

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